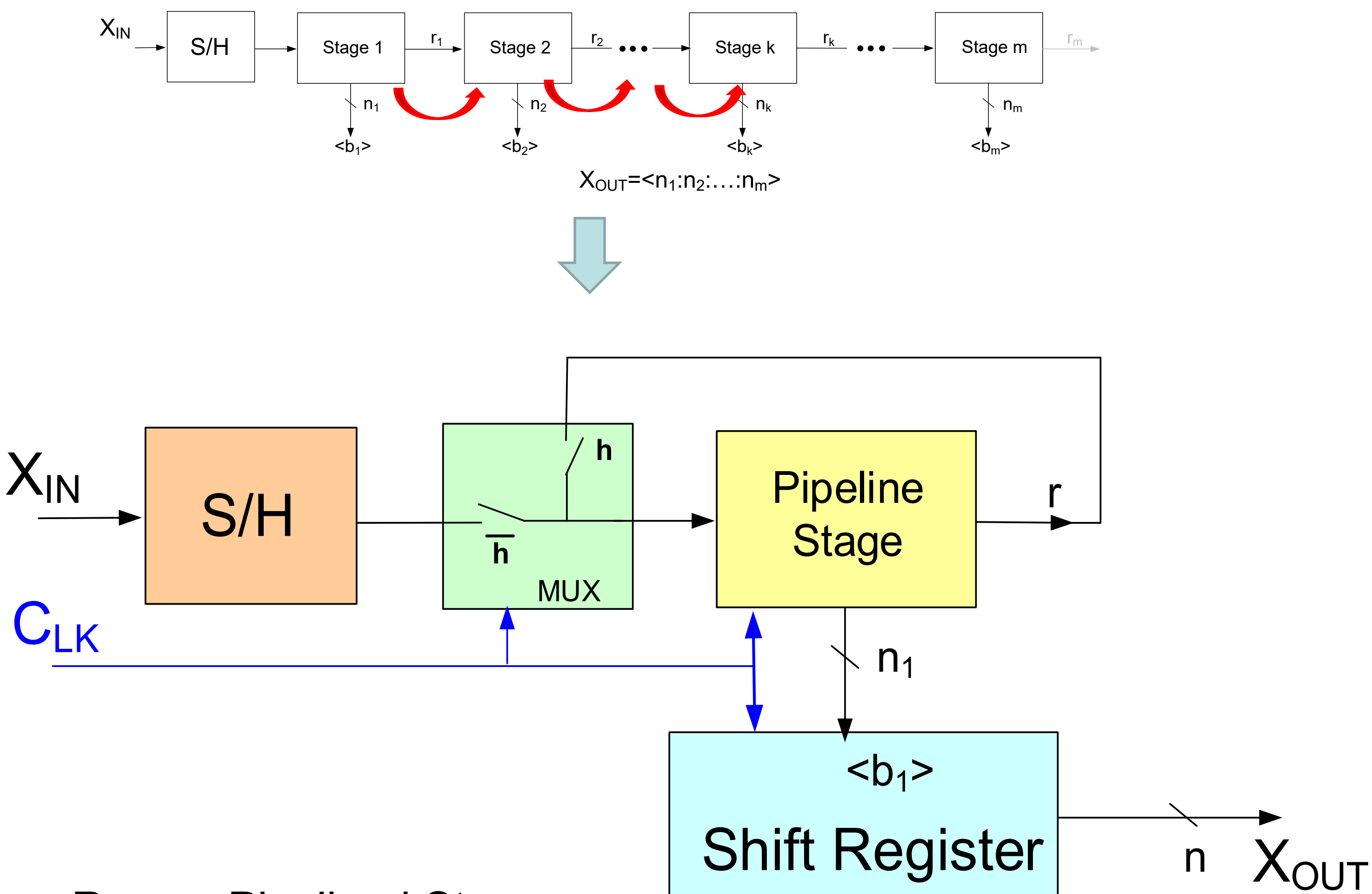
EE 435

Lecture 38

Data Converters

- Noise
- Statistical Characterization

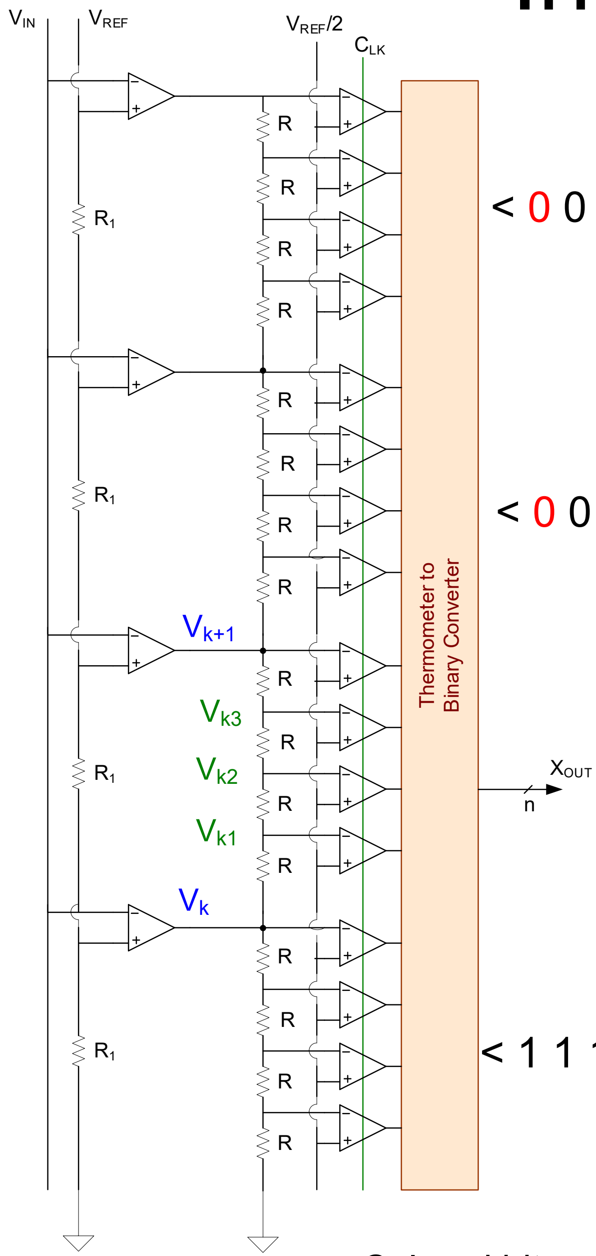
Cyclic (Algorithmic) ADC



- Re-use Pipelined Stage
- Small amount of hardware
- Effective thru-put decreases

Review from Last Lecture

Interpolating ADC

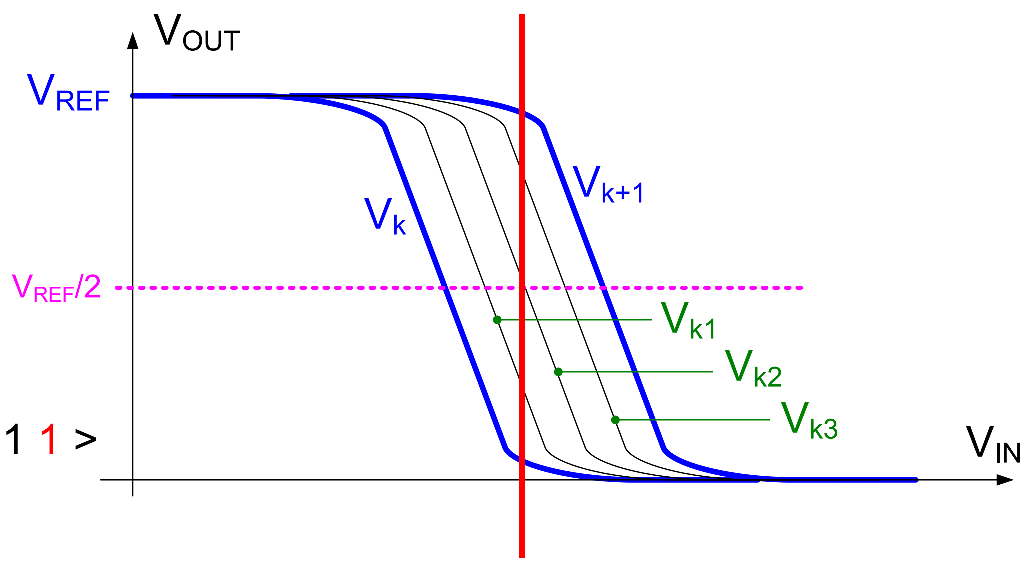


< 0 0 0 0 0 >

< 0 0 0 0 0 >

< 1 1 1 1 1 >

- Amplifiers are finite-gain saturating
- Amplifiers need not be accurate or linear
- Shown for 4-bit
- Same common-mode input on comparators
- Clocked comparators usually regenerative
- Reduces Offset Requirements for Comparators

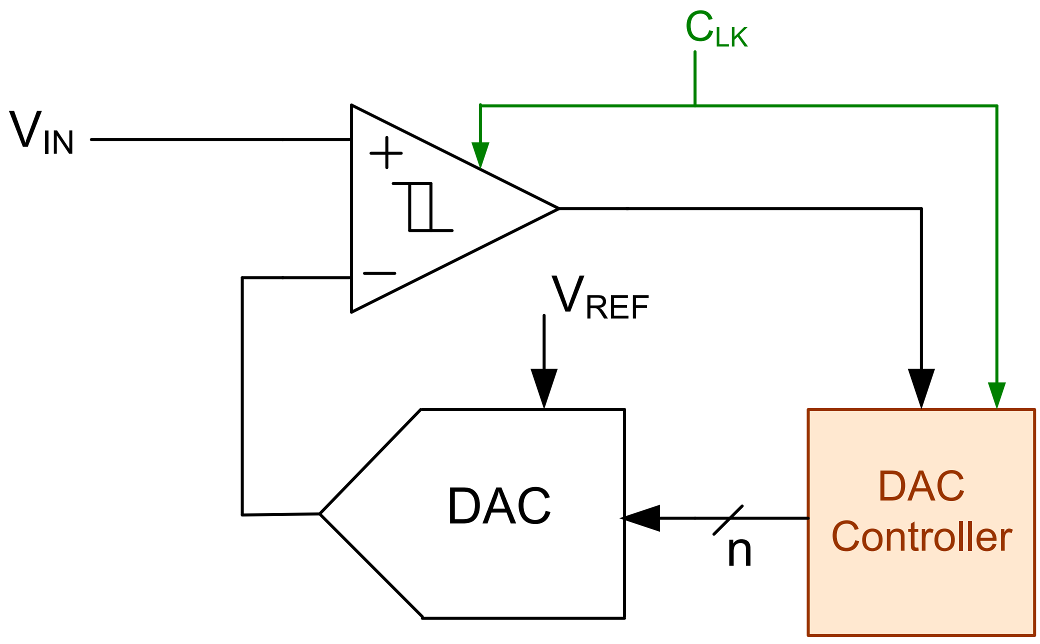


< 1 1 0 0 0 >

Colored bits are shared

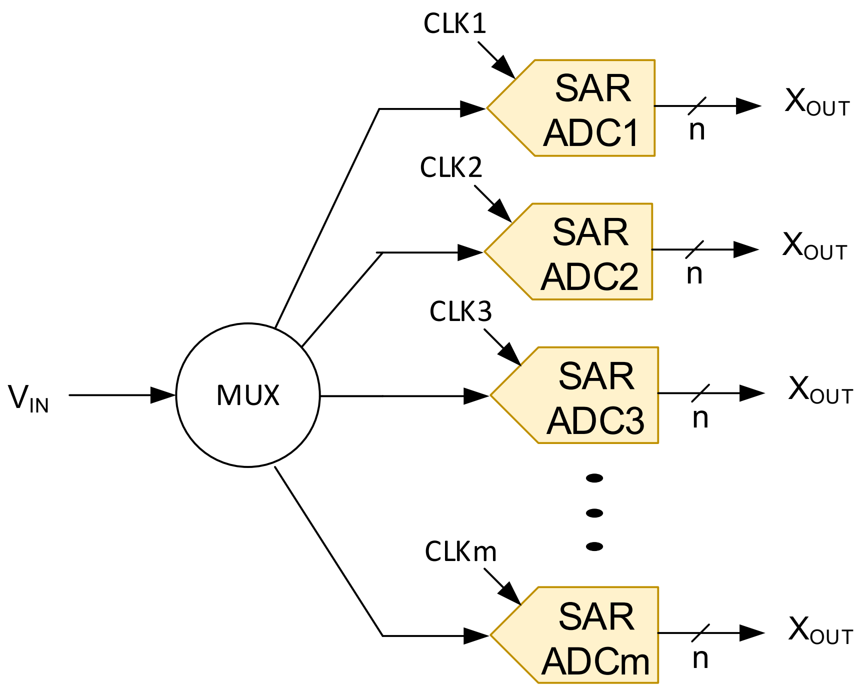
Review from Last Lecture

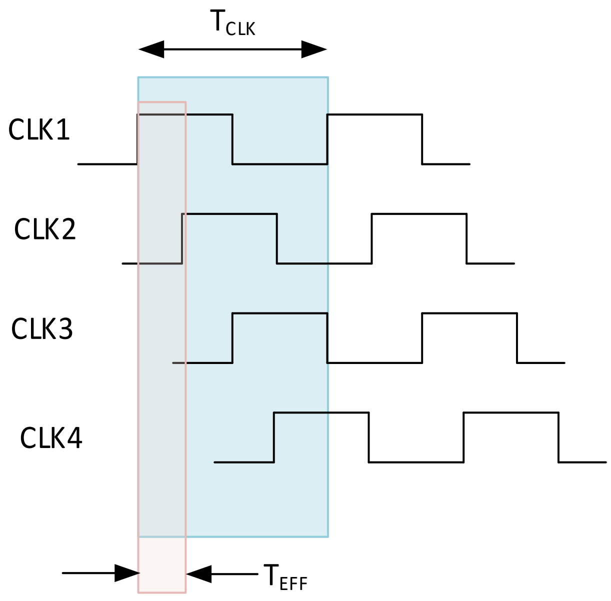
SAR ADC



- DAC Controller may be simply U/D counter
- Binary search controlled by Finite State Machine is faster
- SAR ADC will have no missing codes if DAC is monotone
- Not very fast but can be small
- Any DAC can be used
- Single comparator !

Time Interleaved SAR ADC

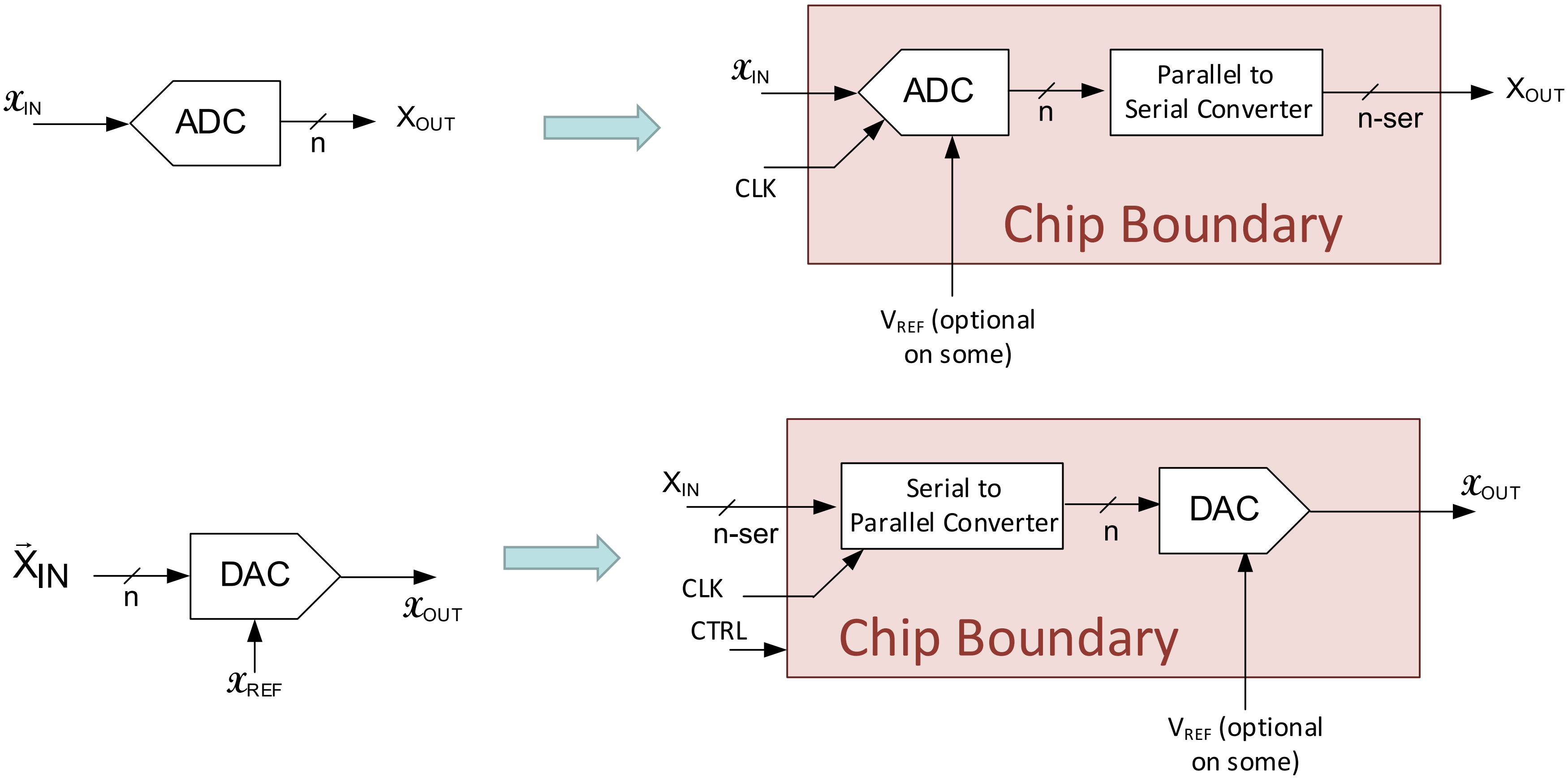




Time interleaving increases effective conversion rate by factor of m

Actual Catalog Data Converter Parts

- Often (not always) digital interface with data converter is serial
- Significantly Reduces pin count
- Interfaces usually follow standard protocols
- Challenge in data converter design almost always in the data converter itself
- Multiple channels often available and these usually use single converter and MUX



Common Application

Want digital representation of analog input at a “distant” location

Distance could be a few cm or thousands of miles

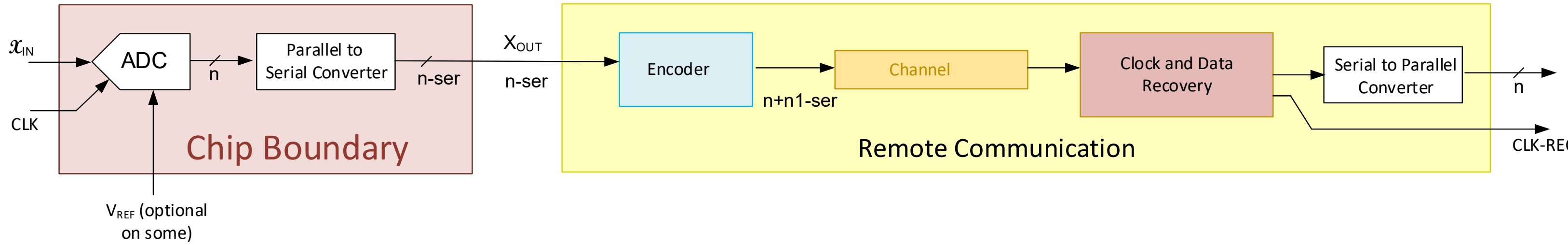
Transmitting clock would dramatically increase communication overhead and provide no additional information

Keeping phase of clock aligned with data would be extremely difficult even for short distances

Data is usually encoded and at receiver end both clock and data are recovered (CDR)

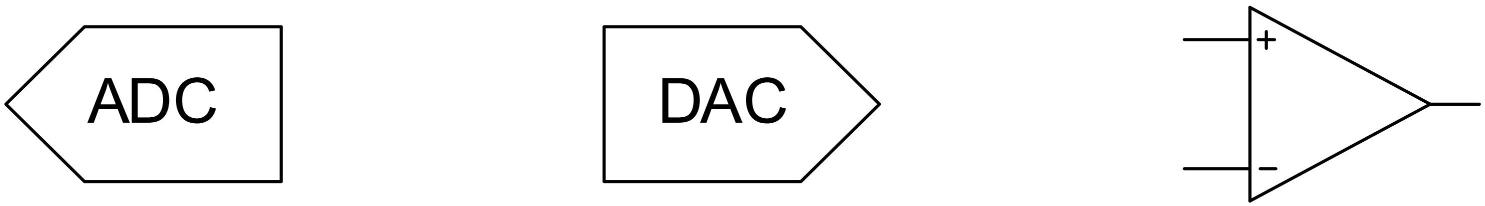
Digital signals themselves degrade when passing through channel

Bit overhead is significant



Typical Serial Communication Application of Data Converter

Noise in ADCs and DACs

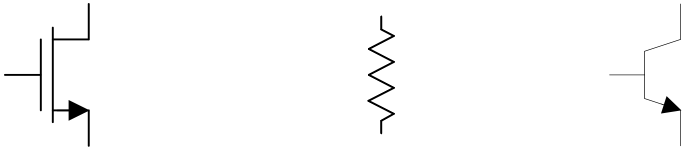


Noise in electronic devices and components introduce noise in electronic systems

Noise is of major concern in ADCs, DADs, and Op Amps

Beyond the scope of this course to go into lots of details about effects of device noise in these components but will provide a brief introduction

Devices that contribute noise :

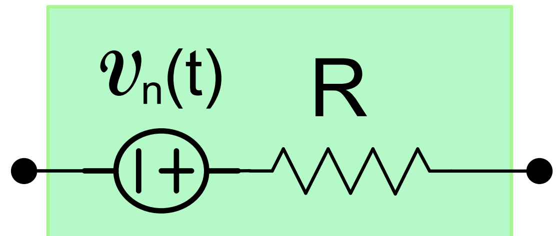


Capacitors and Inductors are noiseless:

Noise in DACs

Resistors and transistors contribute device noise but
what about charge redistribution DACs ?

Noise in resistors:



Noise can be characterized by either $v_n(t)$ (time domain)
or the spectral density S (frequency domain)

Noise spectral density of $v_n(t)$ at all frequencies for a resistor

$$S = 4kTR$$

k: Boltzmann's Constant
T: Temperature in Kelvin

$k=1.38064852 \times 10^{-23}\ m^2\ kg\ s^{-2}\ K^{-1}$

At 300K, $kT=4.14 \times 10^{-21}$

This is termed white noise because S is independent of f !

Noise in DACs

Resistors and transistors contribute device noise but what about charge redistribution DACs ?

Noise in linear circuits:

$$v_n(t) \Longleftrightarrow S(f)$$

Typically interested in RMS value of the noise voltage v_{RMS}

Time domain:

$$v_{RMS} = \sqrt{\lim_{T\to\infty} \frac{1}{T} \int_{t=0}^{T} v_n^2(t)\,dt}$$

Difficult to obtain directly !

Frequency domain:

$$\tilde{v}_{RMS} = \sqrt{\int_{f=0}^{\infty} S(f)\,df}$$

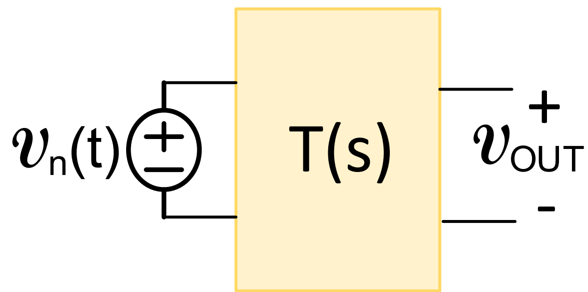
It can be shown that:

$$\tilde{v}_{RMS} = v_{RMS}$$

Noise in DACs

Resistors and transistors contribute device noise but what about charge redistribution DACs ?

Noise in linear circuits:



Due to any noise voltage source:

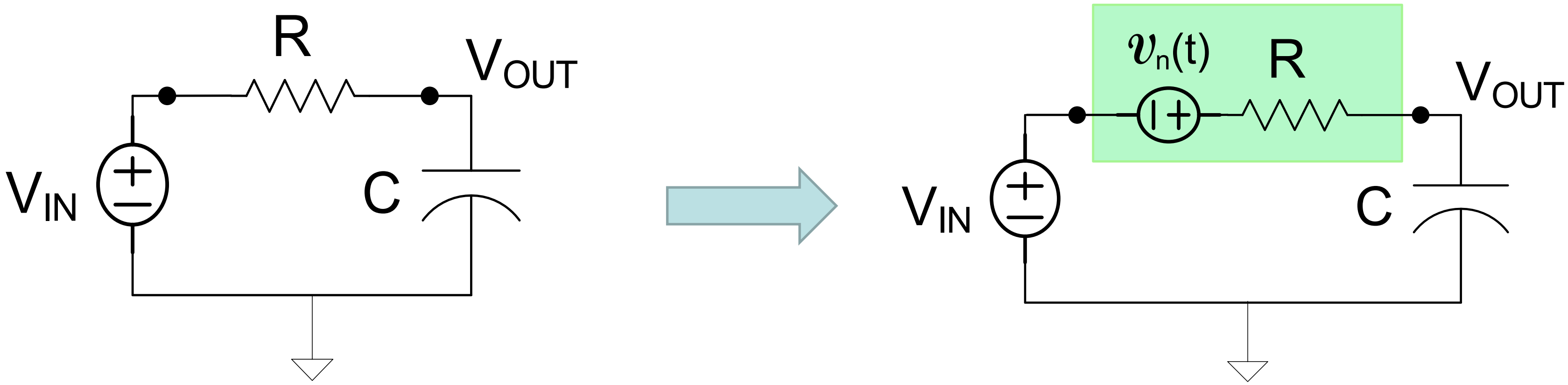
$$S_{V_{OUT}} = S_{V_n} \left| T_n(j\omega) \right|^2$$

$$v_{OUT_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}} \, df}$$

Thus:

$$v_{OUT_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}} \, df} = \sqrt{\int_{f=0}^{\infty} S_{V_n} \left| T_n(j\omega) \right|^2 df}$$

Example: First-Order RC Network



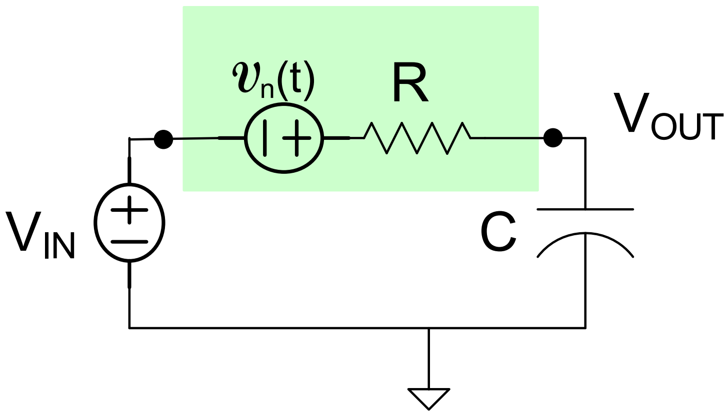
Noise transfer function:

$$T_n(s) = \frac{1}{1+RCs}$$

$$S_{VOUT} = 4kTR\left(\frac{1}{1+(RC\omega)^2}\right)$$

$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{VOUT}\, df} = \sqrt{\int_{f=0}^{\infty} \frac{4kTR}{1+\omega^2R^2C^2}\, df}$$

Example: First-Order RC Network

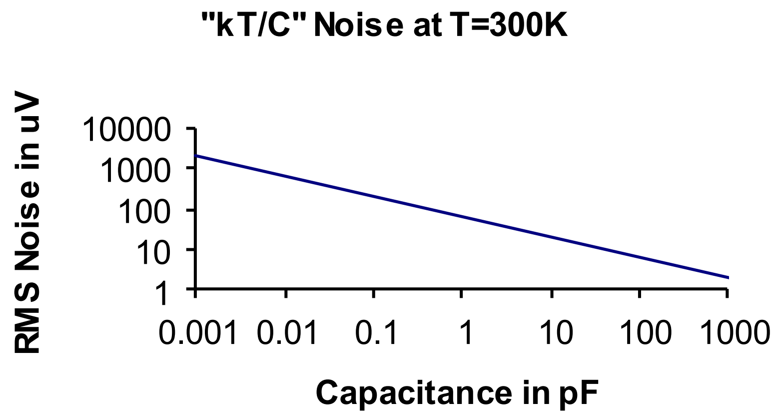


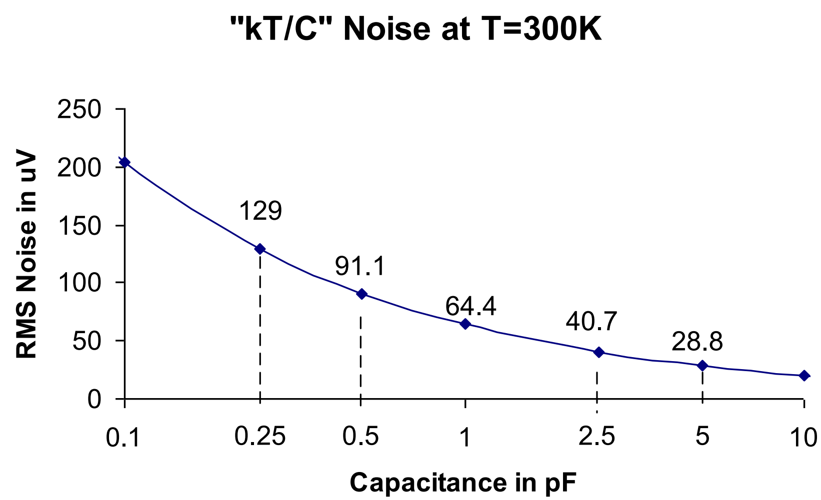
$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\,\mathrm{df}} = \sqrt{\int_{f=0}^{\infty} \frac{4kTR}{1+\omega^2R^2C^2}\,\mathrm{df}}$$

From a standard change of variable with a trig identity, it follows that

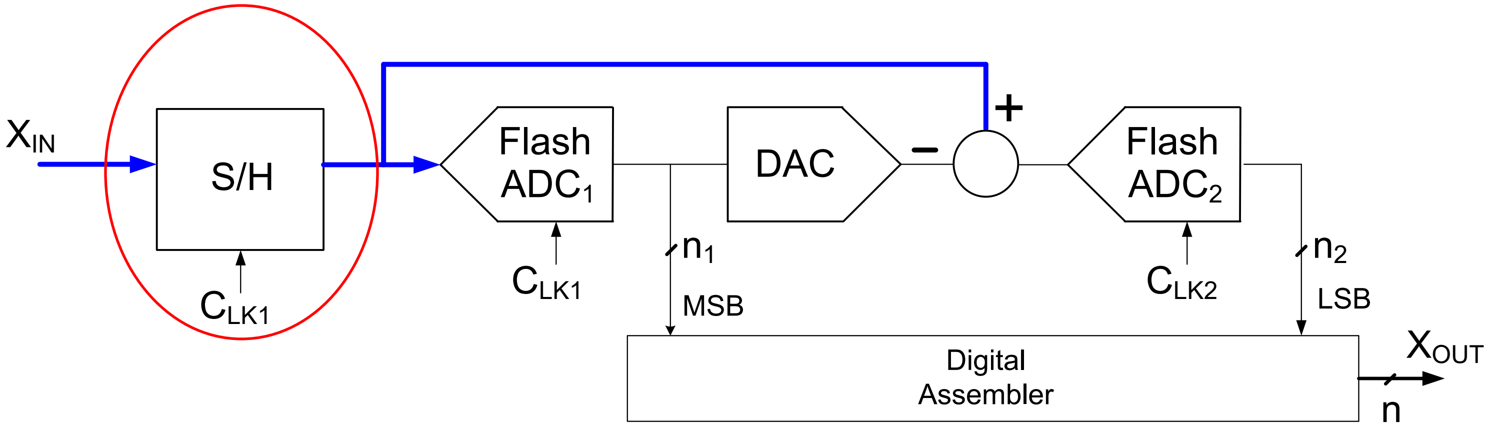
$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\,\mathrm{df}} = \sqrt{\frac{kT}{C}}$$

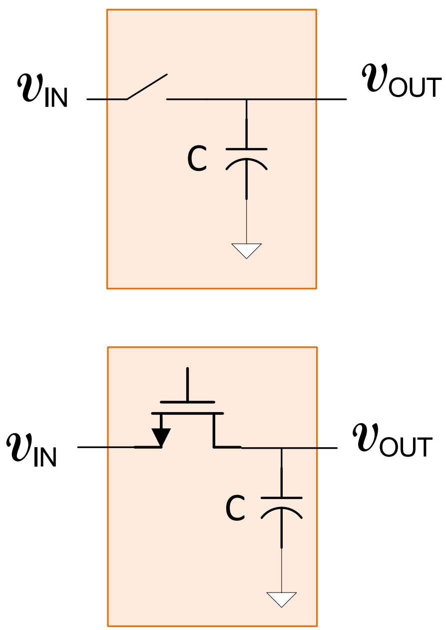
- The continuous-time noise voltage has an RMS value that is independent of R
- Noise contributed by the resistor is dependent only upon the capacitor value C
- This is often referred to at kT/C noise and it can be decreased at a given T only by increasing C


"kT/C" Noise at T=300K
RMS Noise in uV
10000
1000
100
10
1
0.001
0.01
0.1
1
10
100
1000
Capacitance in pF


"kT/C" Noise at T=300K
RMS Noise in uV
250
200
150
100
50
0
129
91.1
64.4
40.7
28.8
0.1
0.25
0.5
1
2.5
5
10
Capacitance in pF

Sample and Hold Circuits





Basic S/H circuit

Slightly more complicated S/H used for input S/H

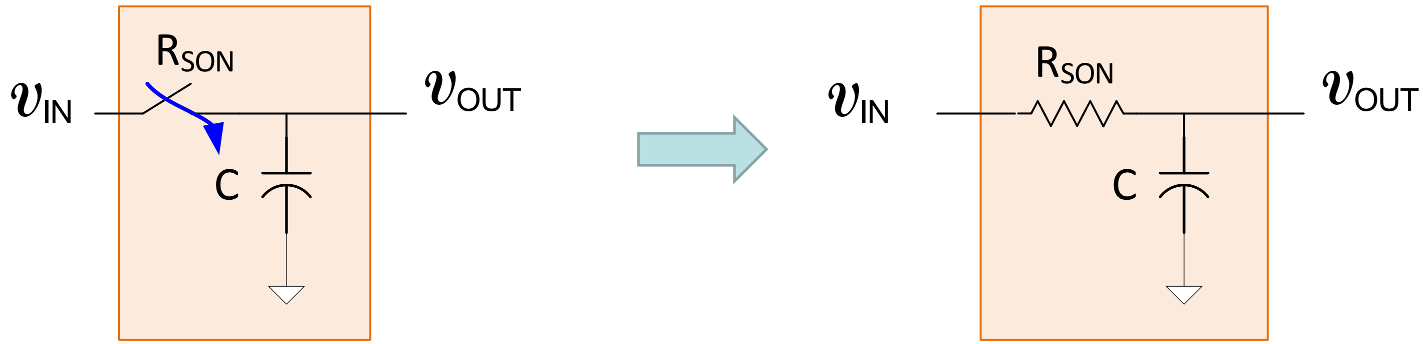
This simple structure used in some applications

Actually a Track and Hold Circuit

Noise characteristics of S/H similar to that of these simple samplers

Sample and Hold Circuits

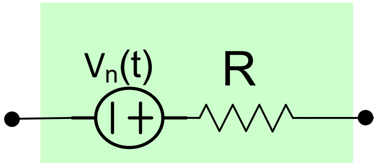
During Track Mode



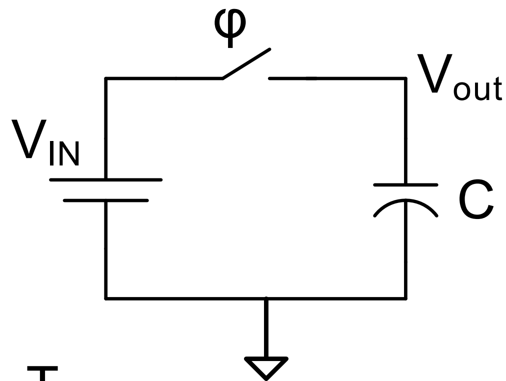
When switch is opened to take sample, noise on C is captured on C (superimposed on signal)

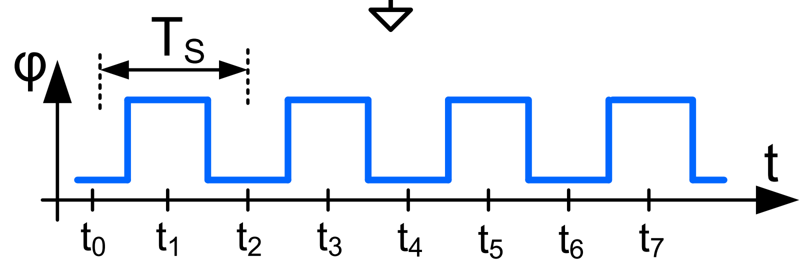
This noise becomes input noise to the ADC

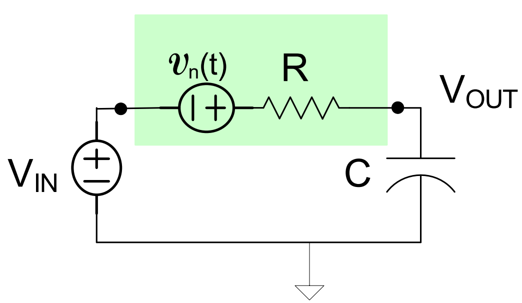
Recall noise in resistor modeled as noise voltage source in series with R



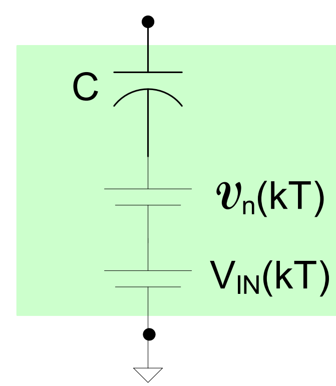
Sample and Hold Circuits







Track mode

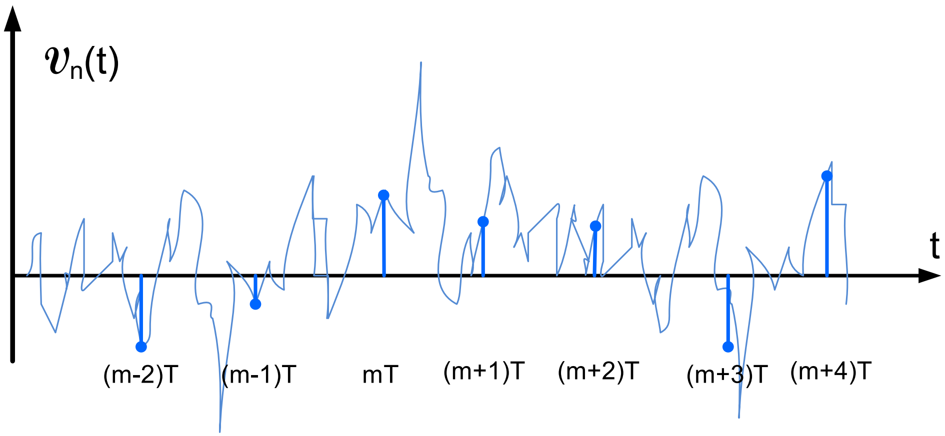


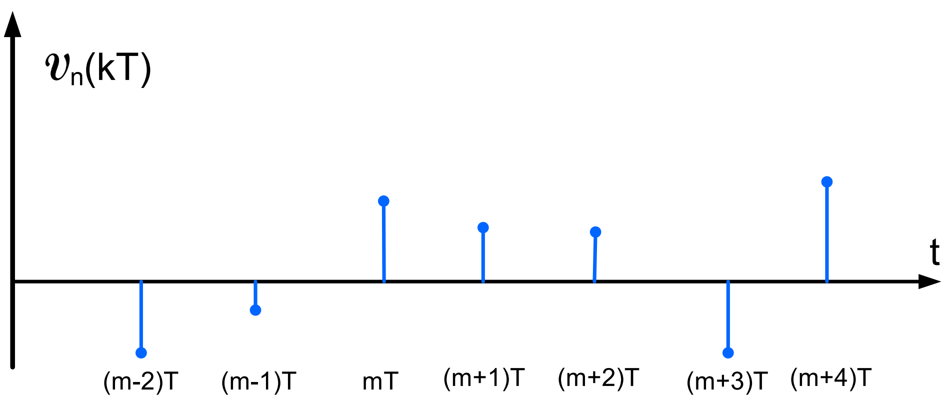
Hold mode

If switch opens fast, noise on C due to R is captured as $v_n(kT)$

Sample and Hold Circuits

T is the period of the sampler

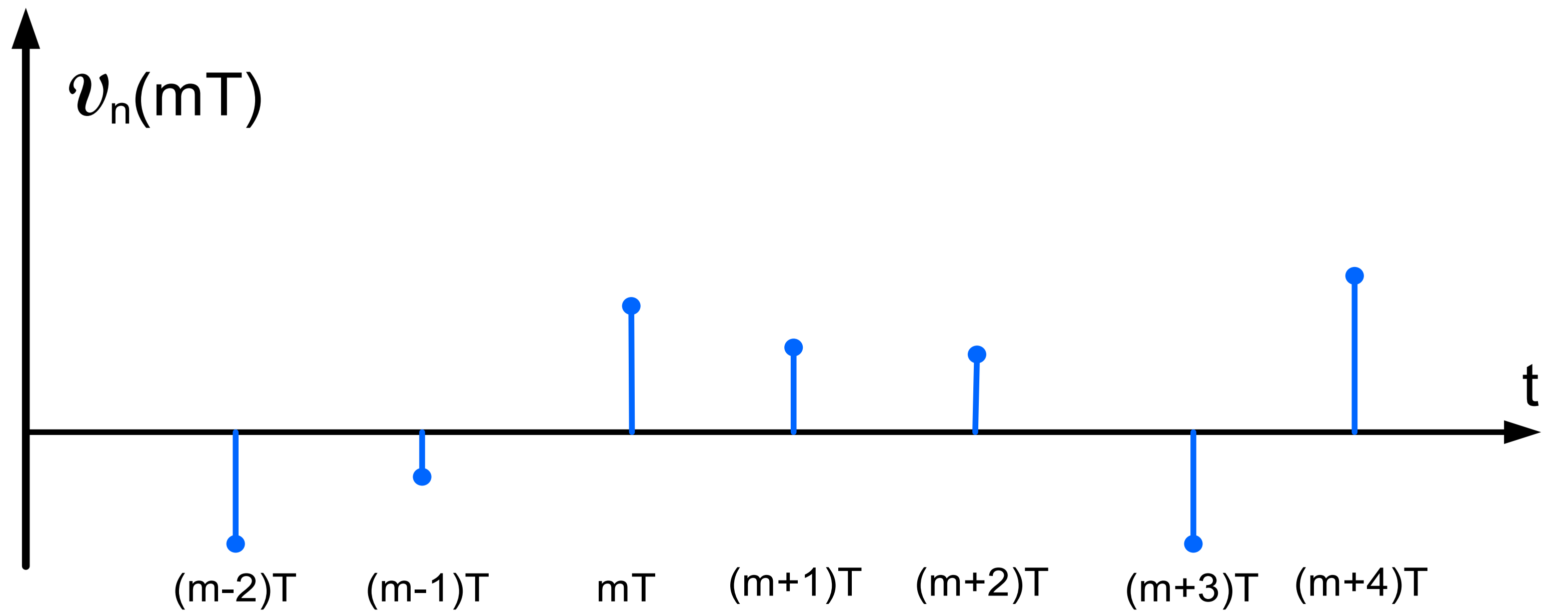




$v_n(mT)$ is a discrete-time sequence obtained by sampling continuous-time noise waveform

RMS value of noise input to pipelined ADC is that of the discrete time noise sequence

Sample and Hold Circuits



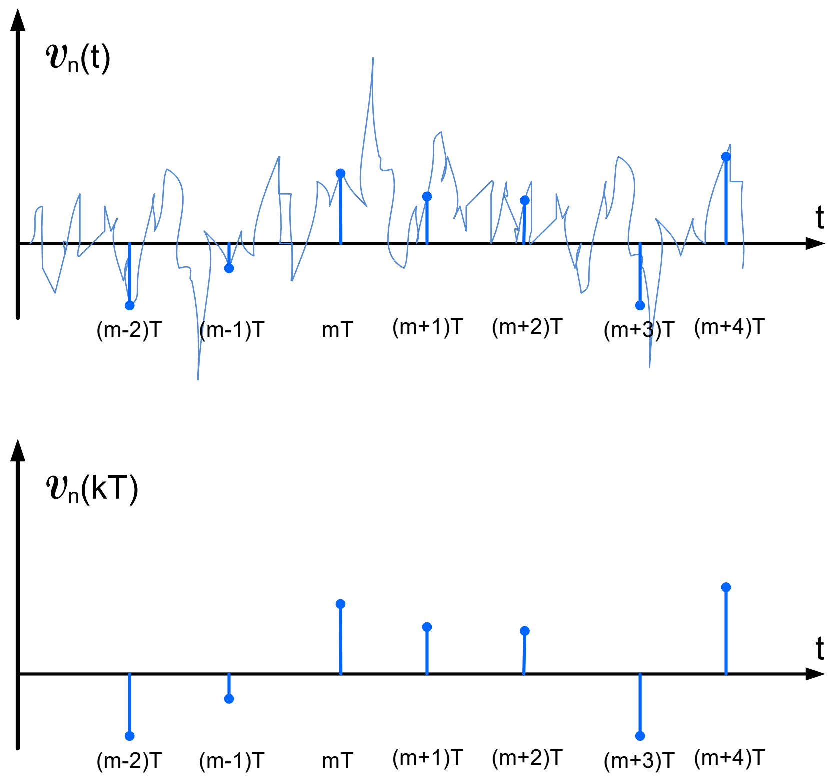
Define the RMS noise of a discrete time noise sequence as

$$\hat{v}_{RMS} = E\left(\sqrt{\lim_{N\to\infty}\left(\frac{1}{N}\sum_{m=1}^{N} v^2(mT)\right)}\right)$$

Thus:

$$\hat{v}_{RMS} = E\left(\sqrt{\lim_{N\to\infty}\left(\frac{1}{N}\sum_{m=1}^{N} v^2(mT)\right)}\right) \underset{N\, large}{\simeq} \sqrt{\frac{1}{N}\sum_{m=1}^{N} v^2(mT)}$$

Sample and Hold Circuits



$v_n(mT)$ for each m is a random variable with some distribution function

This distribution function is independent of m (i.e. the variables are identically distributed)

Assume μ_n is the mean and σ_n is the standard deviation of this random variable

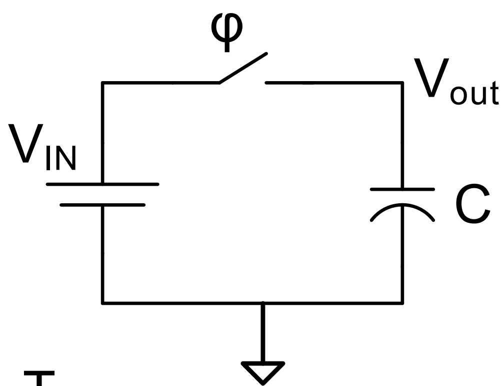
What is the relationship, if any, between $v_{n_{RMS}}$ and $\hat{V}_{RMS}$

Theorem 1 If $\mathcal{V}(t)$ is a continuous-time zero-mean noise source and $<\mathcal{V}(kT)>$ is a sampled version of $\mathcal{V}(t)$ sampled at times T, 2T, …. then the RMS value of the continuous-time waveform is the same as that of the sampled version of the waveform. This can be expressed as $\mathcal{V}_{RMS} = \hat{\mathcal{V}}_{RMS}$

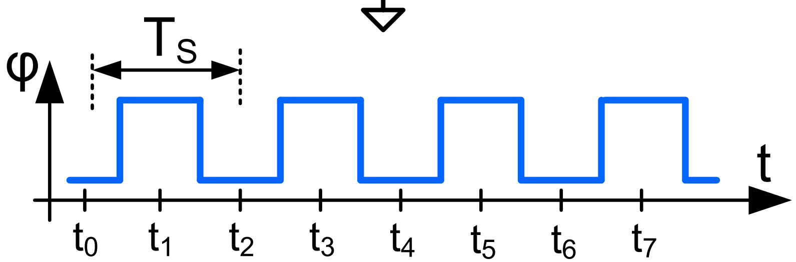
Theorem 2 If $\mathcal{V}(t)$ is a continuous-time zero-mean noise signal and $<\mathcal{V}(kT)>$ is a sampled version of $\mathcal{V}(t)$ sampled at times T, 2T, …. then the standard deviation of the random variable $\mathcal{V}(kT)$, denoted as $\sigma_{\hat{V}}$ satisfies the expression $\sigma_{\hat{V}} = \mathcal{V}_{RMS} = \hat{\mathcal{V}}_{RMS}$

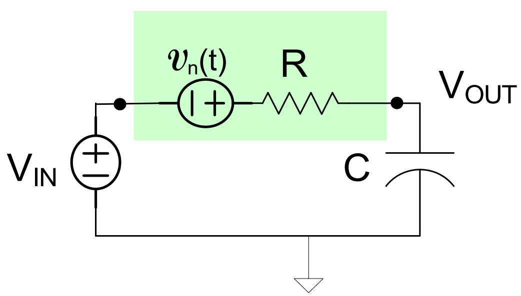
From Theorem 1 we obtain the RMS value of the switched capacitor sampler

Sample and Hold Circuits

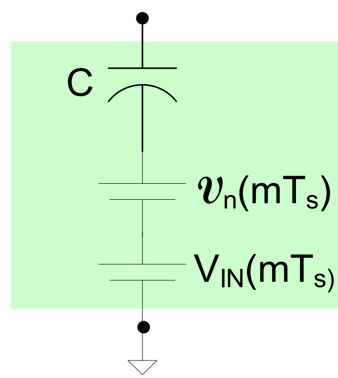


$$v_{n_{RMS}} = \sqrt{\int_{f=0}^{\infty} S_{V_{OUT}}\, df} = \sqrt{\frac{kT}{C}}$$





Track mode



Hold mode

$$v_{n_{RMS}} = \sqrt{\frac{kT}{C}}$$

k: Boltzmann's constant
T: temperature in Kelvin

RMS noise at output of basic SC S/H is independent of R but dependent upon C

Statistical Analysis of Data Converters

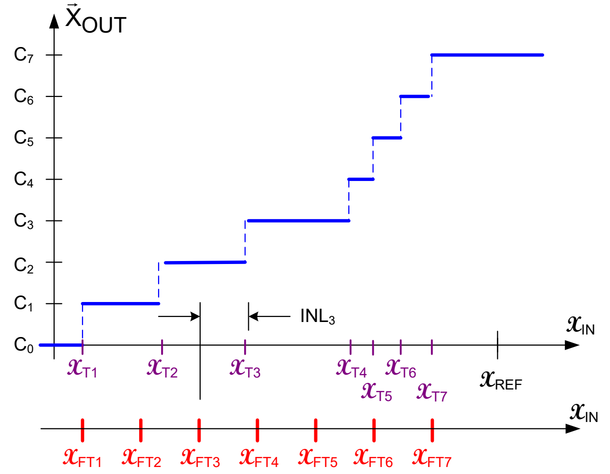
Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition

$$\mathrm{INL_k} = \frac{x_{Tk} - x_{FTk}}{x_{LSB}} \qquad 1 \le k \le N\text{-}2$$

$$\mathrm{INL} = \max_{2 \le k \le N-2} \left\{ \left| \mathrm{INL_k} \right| \right\}$$



- Component dimensions and model parameters of all devices in a data converter are actually random variables at the design stage!
- At design stage, INL characterized by standard deviation of many random variables
- Closed-form expressions for INL almost never exist because PDF of order statistics of correlated random variables is extremely complicated
- Simulation of INL very time consuming if n is very large (large sample size required to establish reasonable level of confidence)
  - -Model parameters become random variables
  - -Process parameters affect multiple model parameters causing model parameter correlation
  - -Simulation times can become very large

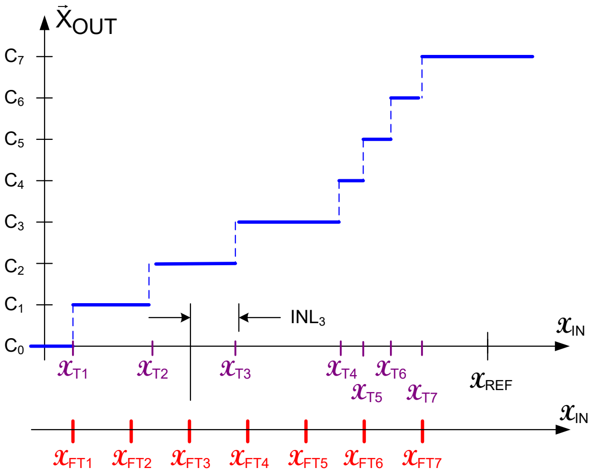
Integral Nonlinearity (ADC)

Nonideal ADC

Break-point INL definition

$$INL_k = \frac{x_{Tk} - x_{FTk}}{x_{LSB}} \qquad 1 \le k \le N-2$$

$$INL = \max_{2 \le k \le N-2} \left\{ \left| INL_k \right| \right\}$$



- INL can be readily measured in laboratory but often dominates test costs because of number of measurements needed when n is large
- Expected value of INL_k at k=(N-1)/2 is largest for many architectures
- INL of $\frac{x_{LSB}}{2}$ often considered acceptable (this is the ideal value of the continuous-input INL definition though many high-speed ADCs and some lower-speed structures will have an INL that exceeds this)

- Major effort in ADC design is in obtaining an INL acceptable yield !
- Yield often strongly dependent upon matching of random variables !

Characteristics of Data Converters Dominantly Depend Upon Random Variables

- Static characteristics
  - Resolution
  - Least Significant Bit (LSB)
  - Offset and Gain Errors
  - Absolute Accuracy
  - Relative Accuracy
  - Integral Nonlinearity (INL)
  - Differential Nonlinearity (DNL)
  - Monotonicity (DAC)
  - Missing Codes (ADC)
  - Quantization Noise
  - Low-f Spurious Free Dynamic Range (SFDR)
  - Low-f Total Harmonic Distortion (THD)
  - Effective Number of Bits (ENOB)
  - Power Dissipation

Characteristics of Data Converters Dominantly Depend Upon Random Variables

- Dynamic characteristics
  - Conversion Time or Conversion Rate (ADC)
  - Settling time or Clock Rate (DAC)
  - Sampling Time Uncertainty (aperture uncertainty or aperture jitter)
  - Dynamic Range
  - Spurious Free Dynamic Range (SFDR)
  - Total Harmonic Distortion (THD)
  - Signal to Noise Ratio (SNR)
  - Signal to Noise and Distortion Ratio (SNDR)
  - Sparkle Characteristics
  - Effective Number of Bits (ENOB)

Methods of Characterizing how Random Variables Affect Performance

- Analytical Statistical Formulation and Analysis
- MATLAB Simulations (often using Monte-Carlo Analysis)
- Spectre/Spice Monte-Carlo Simulations
- Ignore Effects of Random Effects

How important is statistical characterization of data converters?

Stay Safe and Stay Healthy !

End of Lecture 38